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Low-Power, Self-Rectifying, and Forming-Free Memristor with an Asymmetric Programing Voltage for a High-Density Crossbar Application

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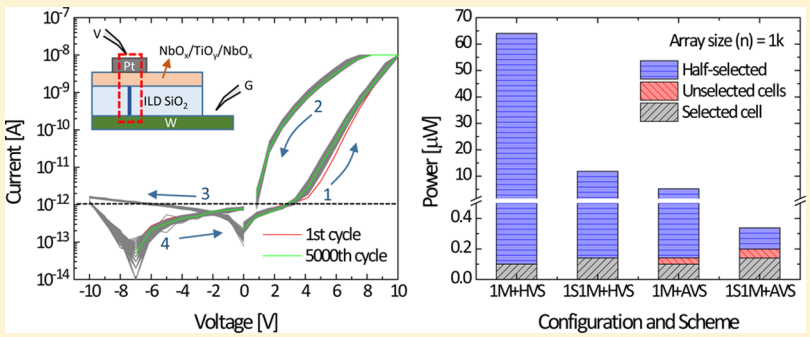
Supporting Information



ABSTRACT: A Pt/NbO_x/TiO_y/NbO_x/TiN stack integrated on a 30 nm contact via shows a programming current as low as 10 nA and 1 pA for the set and reset switching, respectively, and a self-rectifying ratio as high as ~10^5, which are suitable characteristics for low-power memristor applications. It also shows a forming-free characteristic. A charge-trap-associated switching model is proposed to account for this self-rectifying memrisive behavior. In addition, an asymmetric voltage scheme (AVS) to decrease the write power consumption by utilizing this self-rectifying memristor is also described. When the device is used in a 1000 × 1000 crossbar array with the AVS, the programming power can be decreased to 8.0% of the power consumption of a conventional biasing scheme. If the AVS is combined with a nonlinear selector, a power consumption reduction to 0.31% of the reference value is possible.

KEYWORDS: *Low current, low power, self-rectifying, forming-free, memristor*

Resistance-switching memristors composed of transition-metal oxide are promising electronic components for a variety of future applications because of their nonvolatile and reversible conductance change in response to an applied stimulus.[1,2] These characteristics make memristors applicable to high-density nonvolatile memory as well as emerging stateful logic and bioinspired neuromorphic devices.[3−8] These applications require very low power consumption to compete with complementary metal oxide semiconductor field-effect transistors in conventional memory and logic circuits.[9,10] Even though numerous memristor materials have been proposed over the past decade,[11] only a few studies have demonstrated low-power operation,[10,12−17] which has proven to be challenging. In many cases, repeatable memristive switching behavior is preceded by an electroforming step, which forms a localized conducting channel[18] that should have a value higher than a half-integer quantum conductance ($1/2G_0 = e^2/h = \sim 3.9 \times 10^{-5}$ S) to reach a stable ON state.[19,20] In this case, assuming the reset voltage (V_{RES}) is 1 V, the reset power ($P_0 = V_{RES}^2 \times 1/2G_0$) to shut off this single contact channel is ~39 μW, which corresponds to the minimum achievable operating power in this specific case. Therefore, it is important to explore memristor materials and structures that can be operated in the insulating regime without the formation of a conducting channel to attain low-power operation.

In addition, a memristor should be self-rectifying for crossbar applications to achieve a small feature size and high storage density.[7,21,22] The well-known sneak current issue must be

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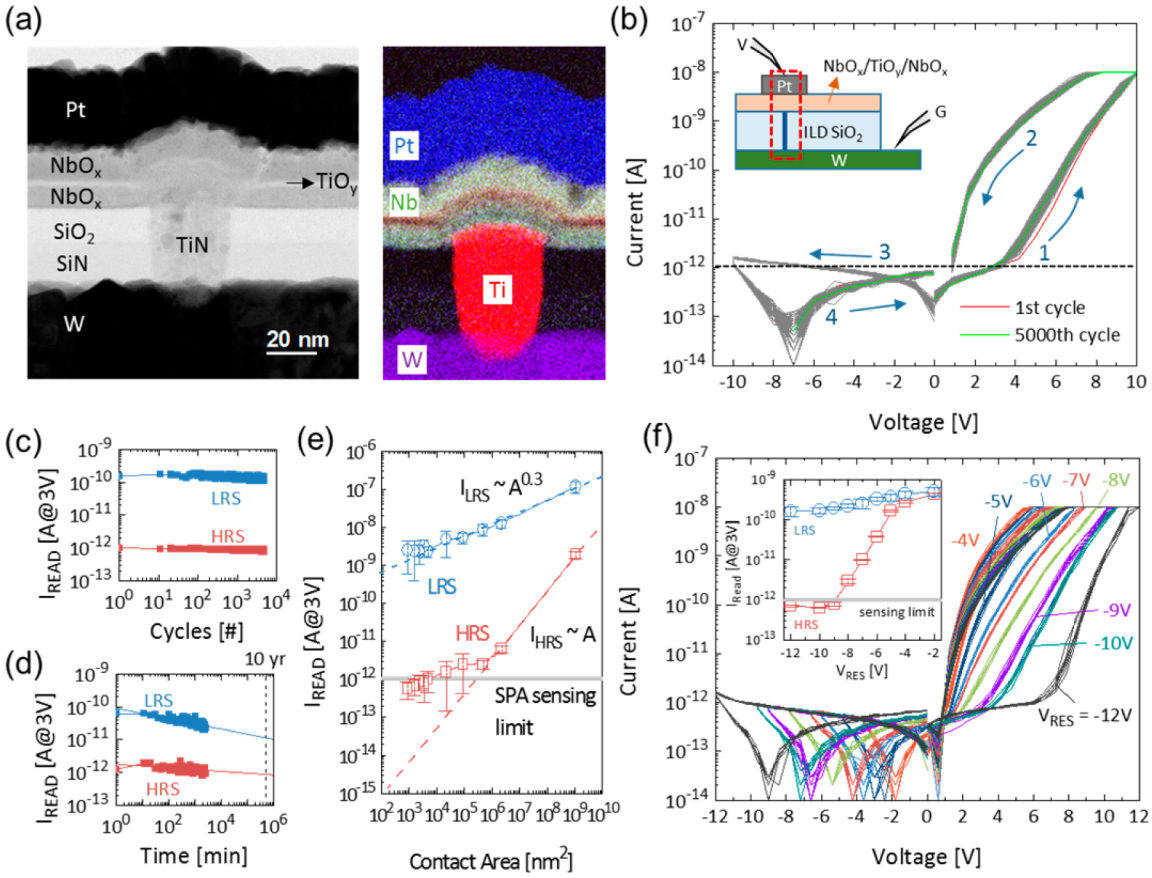

Figure 1. Pt/NbO_x/TiO_y/NbO_x/TiN memristor device. (a) The cross-sectional transmission electron microscope (TEM) image of the device. The right panel shows the electron energy-loss spectroscopy (EELS) mapping image for heavy-metal elements. (b) The resistance switching $I-V$ curves of the device with a 10 nA set compliance current (I_{CC}). The inset schematically shows the testing setup for the measurement. (c) The cycling stability read at 3 V for 5000 cycles in a DC sweep mode. (d) The retentions of the LRS and HRS at room temperature. (e) The area-dependent read current at the same switching conditions. The I_{CC} was not utilized during this test. (f) The reset voltage-dependent $I-V$ curves with a 10 nA I_{CC}. The inset shows the read current at 3 V as a function of the reset voltage.

appropriately addressed; otherwise, it can overwhelm data sensing during reading and increase the power consumption during programming.[23] For the resolution of this sneak current problem, inserting a selector component into the memory cell is an effective solution. However, developing a high performance selector device is still a challenging task.[24,25] In this regard, a memristor with a self-rectifying characteristic can offer a huge benefit over a cross-point cell composed of separate memory and selector devices.

In this paper, a low current and self-rectifying Pt/NbO_x/TiO_y/NbO_x/TiN memristor is described. The device showed a programming current as low as 10 nA and 1 pA for the set and reset switching, respectively, and a self-rectifying ratio as high as $\sim 10^5$, which are suitable characteristics for low-power memristor applications. Although the rectification behavior of a diode selector has been regarded as a feasible method by which to alleviate read disturbance, its possible use in decreasing write power consumption has not been addressed. In this study, however, an optimized programming scheme to decrease the write power consumption by utilizing this self-rectifying memristor is also described.

To fabricate the Pt/NbO_x/TiO_y/NbO_x/TiN memristor, a blanket W layer was deposited by chemical vapor deposition (CVD) on a SiO_2/Si substrate. Then, 50 nm thick SiO_2 was deposited, and various diameters of contact holes from 30 nm to 2 μm were patterned through the SiO_2 layer by photolithography. TiN for the bottom electrode vias was deposited by CVD followed by chemical mechanical polishing. Then, 10 nm NbO_x, 2 nm TiO_y, and 10 nm NbO_x were sequentially deposited by atomic layer deposition (ALD) at 300 °C by using the metal−organic compounds (*tert*-butyl)tris(methylethylamino)nibioum (TBTMEN) and tetrakis(diethylamido)titanium (TDEAT) for Nb and Ti precursors, respectively, and remote O_2 plasma for the oxygen source. X-ray photoelectron spectroscopy (XPS) results confirmed that this film contained NbO_x and TiO_y, where the NbO_x was composed of ~60% Nb_2O_5 and ~40% NbO_2 (see Figure S1). Note that the binding energy of Ti 2*p* from the device matches that of titanium oxide rather than metallic titanium, suggesting oxidized Ti. For the XPS analysis, the sample was sputter-cleaned for 2 min using Ar gas so that a relatively higher amount of TiO_y (~22%) was detected than the deposited film thicknesses (~9.1%). Then, a 30 nm thick Pt (or TiN) top electrode was deposited by sputtering through a shadow mask. A cross-sectional transmission electron microscope (TEM) specimen was made using a FEI Helios dual beam system. Aberration-corrected scanning electron transmission microscopy−electron energy-loss spectroscopy (STEM−EELS) analysis was performed using a FEI Titan TEM at an accelerating voltage of 300 kV. For the electrical testing, an Agilent 4156C Precision Semiconductor Parameter Analyzer was used for the DC electrical characterizations. During the electrical measure-

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ments, the Pt (or TiN) top electrode was biased while the W bottom electrode was grounded.

Figure 1a shows a cross-section TEM image of the Pt/NbO_x/TiO_y/NbO_x/TiN (P-NTN) device (left panel) formed on a 30 nm diameter contact via. The right panel of Figure 1a shows the EELS mapping image for heavy metal elements, which clearly shows the elemental distribution inside the device. Figure 1b shows the current−voltage ($I-V$) characteristics for 5000 cycles with a 10 nA set compliance current (I_{CC}), where the first and 5000th $I-V$ sweep curves are highlighted with red and green lines, respectively. The inset shows the schematic of the cross-section of the device during the electrical testing, where the red rectangular area corresponds to the TEM image of Figure 1a. This device was electroforming-free, and its virgin state was a high-resistance state (HRS). From the virgin state, the first voltage sweep (which corresponds to the first set switching) was performed by applying a positive bias on the Pt top electrode from 0 to 10 V with a 10 nA I_{CC}, which changed the resistance state from the HRS to the nonvolatile low-resistance state (LRS). A negative voltage sweep was performed from 0 to −10 V, which reset the device to the HRS. Subsequent switching cycles were repeated under the identical set and reset conditions. A black dashed line at 1 pA indicates the nominal sensing limit of the semiconductor parameter analyzer (SPA). The butterfly shape of the $I-V$ behavior in the negative voltage range is associated with the noise from the SPA rather than any state change of the devices (see Figure S2). Figure 1c shows the cycling stability in DC sweep mode, where the read current at 3 V (I_{READ}) was recorded for 5000 cycles. This read voltage was carefully chosen to make the read current higher than the sensing limit of the apparatus, but even a slightly higher read voltage of 4 V yielded qualitatively the same cyclic stability data, indicating that neither voltage was too high to disturb the resistance state. In this device, the switching current was much lower than that of oxygen-ion-migration memristors (typically over ∼μA), which suggests that this low switching current could not trigger the ion movement during switching. As will be discussed later, the resistance switching in this device was likely mediated by electron trapping and detrapping, where oxygen vacancies in the central TiO_y layer, Ti-impurity centers, or both in the NbO_x layer close to the top Pt electrode play the role of trap sites. Because an extremely small switching current and associated power were used during this process, the trap configuration remained invariant during the switching, and, thus, very uniform switching and endurance can be achieved. In addition, because of the forming-free characteristic, highly uniform cell-to-cell and device-to-device characteristics can be achieved (see Figure S3). Meanwhile, the state retention of this device showed that the conductance of the LRS decreased over time (Figure 1d), suggesting that carriers were being captured with time at room temperature. Even in the HRS, there could be residual trap sites that capture the carriers, resulting in the further decrease of conductance over time. However, there is a clear read margin between the LRS and HRS from the extrapolated lifetime of 10 years at room temperature. Figure 1e shows the read current (I_{READ}) of the LRS and HRS, measured at 3 V, as a function of the contact area under the same switching conditions (see Figure S4a). For this experiment, I_{CC} was not utilized to reveal the area scaling effect; therefore, the set current was slightly increased compared to Figure 1c,d. Because the switching in this device is voltage-controlled and thus associated with the electric field, the fixed switching voltages without the I_{CC} can result in both saturated LRS and HRS at given areas. For areas smaller than $\sim 10^5$ nm^2, the I_{READ} in the HRS was below the sensing limit of the semiconductor parameter analyzer. However, for areas larger than $\sim 10^5$ nm^2, the I_{READ} in the HRS was proportional to the area ($I_{READ} \approx$ area), which implies that the electrical conduction occurs uniformly across the entire contact area. However, the I_{READ} in the LRS was proportional to the 0.3th power of the contact area ($I_{READ} \approx \text{area}^{0.3}$), which indicates that the carrier detrapping process was active at restricted regions rather than the entire area. In several memristor devices reported in the literature, the LRS current was constant and thus independent of the area because the current flowed through a localized conduction channel or filament.[3,26,27] Usually, those filaments were formed during an electroforming process at either a locally defective area, such as a grain boundary or an edge of the electrode due to a fringing field. In contrast, the P-NTN device in this work was a forming-free device, which means that no preferential conduction paths were created. However, because of the very small area in contact with the blanket film, a fringing field may enhance the detrapping process along the edge of the device so that the above-mentioned area-dependency of the LRS is achieved. Because of the difference in the area dependence of the LRS and HRS, this material system showed a higher on-to-off ratio as the contact size became smaller, which implies that scaling of the device to smaller sizes should be favorable.

During the reset process in the negative bias region, there was no observable current variation in the $I-V$ curve because the current was below the minimum sensing level (∼1 pA) across the entire voltage region. This corresponds to a system in which an intrinsic selection function (in this case diode-like) was implemented along with the memory cell (self-rectifying functionality), which is a critically important aspect for integration into a crossbar circuit. Nonetheless, identifying the reset threshold voltage was important in this study because it also defines the maximum applicable voltage allowed across the unselected cells during crossbar operation without deleting stored data. To identify the reset threshold, the reset switching voltage was varied from −2 to −12 V while the set voltage was fixed at 10 V with a 10 nA I_{CC}, with the resulting data shown in Figure 1f. The inset of Figure 1f summarizes the I_{READ} using a constant read voltage of 3 V of the LRS and HRS as a function of the reset voltage. It shows that the I_{READ} of the HRS started to decrease at −5 V (which corresponded to the reset threshold voltage), and then it decreased exponentially with more-negative reset voltage. Also, the I_{READ} of the LRS decreased slightly with the increase of the reset voltage amplitude, even with the same set switching conditions. This can be understood as follows: when the reset switching was partially performed so that there were some remaining empty trap sites in the HRS, the following set switching yielded a higher concentration of empty traps even under the identical set-switching conditions, making the LRS more electrically conductive. This is consistent with the I_{CC} dependence on the LRS, where the increase of I_{CC} makes the LRS more conductive (see Figure S4b). This interpretation can be better understood from the electronic switching mechanism discussed below.

Taken together, the combined electrical characteristics in Figure 1, i.e., electroforming-free, high endurance, moderate retention time, low current, and area dependency, indicate that the trapping and detrapping of carriers were responsible for the resistance switching. Although some ionic resistance switching devices have exhibited electroforming-free behavior after

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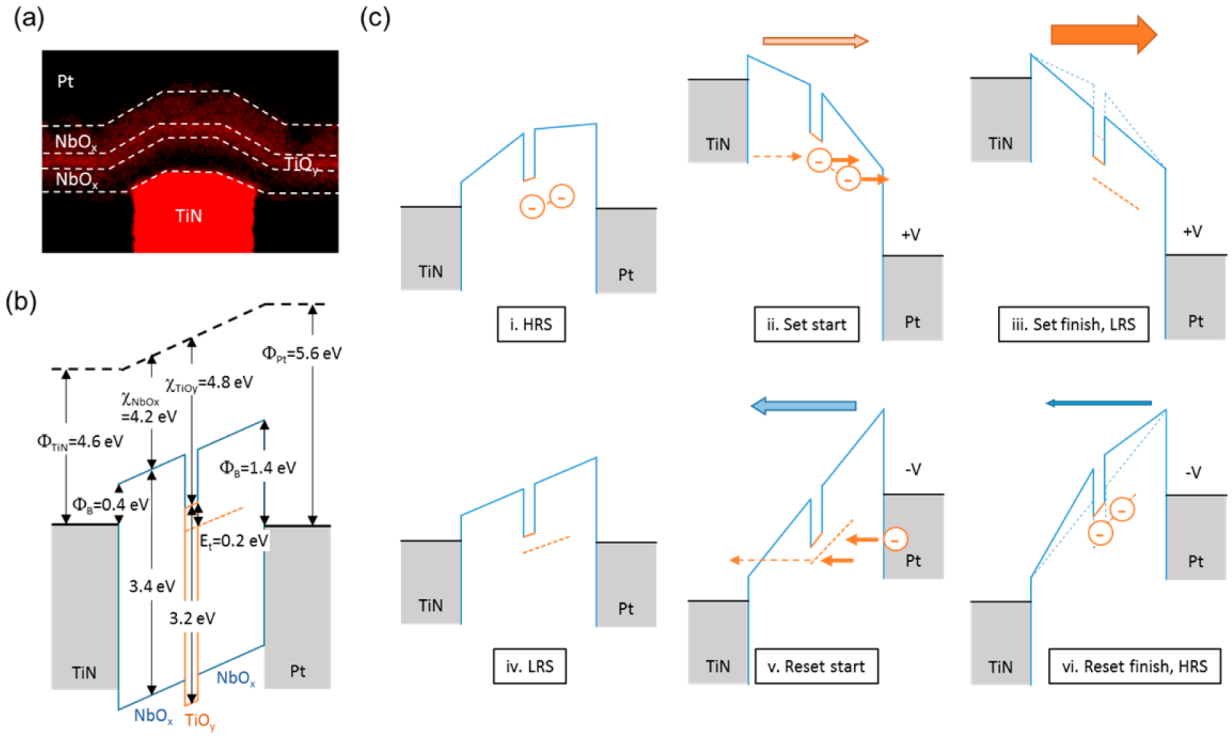

Figure 2. Resistance switching mechanism of the device. (a) The EELS mapping image for Ti. (b) The schematic energy band diagram of the device. (c) The illustration of the charge trapping and detrapping processes in the device. In the HRS, trap sites are filled with electrons (i). When a positive set bias is applied on the Pt electrode (ii,iii), the trapped electrons can be released to the Pt electrode, and the LRS is achieved (iv). When a negative reset bias is applied (v,vi), the Pt electrode can provide the electrons to the trap sites, and the HRS is restored.

accurate control of the oxygen vacancy concentration, those embedded oxygen vacancies tended to increase the leakage current, and therefore, the current level of those devices was not as low as the present device.[13,28] In addition, in several Pt/TiO_2/Pt structures, the bipolar electronic resistance switching has been interpreted in terms of the trapping and detrapping of the carriers into oxygen vacancies associated with ruptured filaments in TiO_2.[29,30] Furthermore, Yoon et al. reported forming-free and highly rectifying memristor switching behavior in Pt/Ta_2O_5/HfO_x/TiN and Pt/Ta_2O_5/HfO_x/Ti structures,[31,32] where the trapping and detrapping of carriers in HfO_x was responsible for the resistance switching, and the Ta_2O_5 layer provided the system with an asymmetric potential barrier that was responsible for self-rectifying. In those cases, the LRS and HRS have been attributed to the trap-filled and trap-empty states, respectively, where the current is commonly described by space-charge limited conduction[29,30] or Poole–Frenkel transport.[31,32]

The switching behavior in the P-NTN device can be understood by a rather different mechanism, although traps inside the insulating layer still play the critical role for the electronic switching. Figure 2a shows the EELS mapping of Ti within the cross-section of the device, where a significant concentration of Ti is observed in the upper NbO_x layer, in addition to that in the central TiO_y layer, whereas in the lower NbO_x layer, Ti is below the detection limit of the EELS. This is likely related with the film growth process. When the TiO_y layer is grown, some partially reacted Ti, perhaps as interstitials, may be present. When the subsequent NbO_x is grown on top, the metastable Ti diffuses into this layer and forms the charge traps responsible for the electronic switching. The Ti associated traps in the TiO_y and upper NbO_x layers, which are located 0.2 eV below the TiO_y conduction band edge,[33] can capture or release carriers through tunneling from and to the Pt electrode according to the bias conditions. Figure 2b shows a schematic energy band diagram of the P-NTN device after thermal equilibrium is established, where the work functions (Φ) of TiN and Pt are assumed to be 4.6 and 5.6 eV, respectively; the electron affinity (χ) and the bandgap (E_G) of NbO_x are 4.2 and 3.4 eV;[34] and those of TiO_y are 4.8 and 3.2 eV, respectively.[35] The χ and E_G values of both NbO_x and TiO_y are taken from the crystalline phases of Nb_2O_5 and TiO_2, and therefore, the actual values may differ from the values used in the diagram. In this band structure, the Ti associated trap energy level in the upper NbO_x layer can be as deep as 0.8 eV if it holds the trap energy level constant. A trap depth of 0.8 eV is enough to provide a reasonable state stability, as shown in Figure 1d for both the trap-filled state and trap-empty state as long as the applied voltage is zero. Although the barrier heights at the TiN–lower NbO_x and Pt–upper NbO_x interfaces may differ from the ideal values estimated from the work functions of the metals and electron affinities of the contacting insulators (~0.4 and ~1.4 eV, respectively), due to interface traps and other factors, it is still reasonable to expect that the former has a significantly lower value than the latter. This means that the carrier trapping and detrapping at the trap centers in TiO_y at low or no bias occur primarily through the exchange of electrons with TiN rather than Pt. The presence of a significant trap concentration near the Pt electrode, however, may have a more critical influence on the charge trapping behavior at voltages higher than the barrier height difference, which then determines the resistance values at lower voltages. Figure 2c shows the change of the band diagram during the switching process. Panel i shows the pristine state, which corresponds to the HRS. In this

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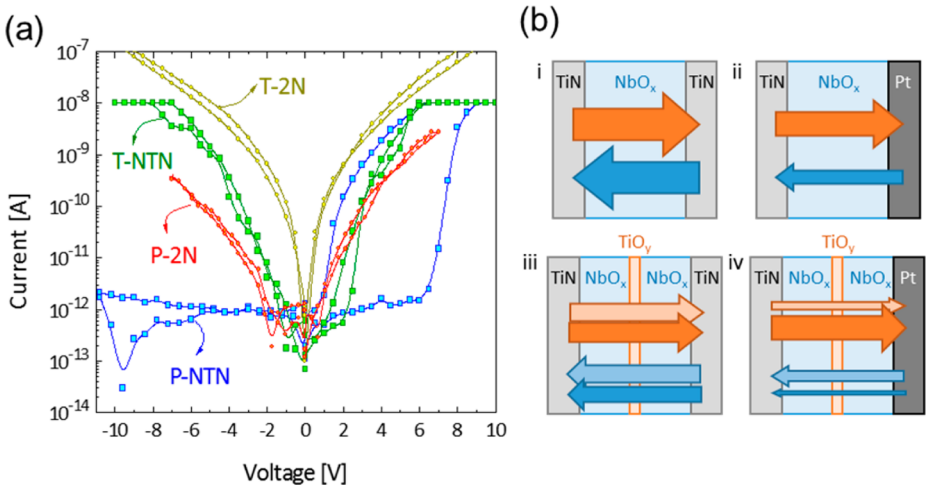

Figure 3. (a) The $I-V$ curves of TiN/NbO_x/TiN (T-2N), Pt/NbO_x/TiN (P-2N), TiN/NbO_x/TiO_y/NbO_x/TiN (T-NTN), and Pt/NbO_x/TiO_y/NbO_x/TiN (P-NTN) devices. (b) The schematic illustration of the conduction in the devices of (a). Upper and lower double arrows in panels iii and iv represent the current flow for low and high voltage bias amplitudes, respectively.

pristine state, the trap sites are already filled with electrons because they are lower than the Fermi energy, and the device experienced a 300 °C temperature during fabrication that populated the states. As the retention trace of this device (Figure 1d) shows, the HRS is energetically more stable than the LRS, so the LRS decays to the HRS given enough time even at room temperature. Because of the presence of rather high Schottky barriers at both the TiN−lower NbO_x and Pt−upper NbO_x interfaces, current flow under an applied bias can occur via either thermionic emission or (trap-assisted) tunneling (or both). When the electrons are trapped in the trapping centers, the resulting negative space charge increases the effective Schottky barrier height and width, and thus, the electron transport is decreased for both bias polarities. When a positive set bias is applied on the Pt electrode (panels ii and iii), the trapped electrons can be released to the Pt electrode because the Fermi level of the Pt electrode is pulled low: the space charge disappears, the current level increases, and the LRS is achieved. There can also be a trapping process from the TiN electrode to the trap sites, but this process is negligible compared to the detrapping process because of the longer tunneling distance between the TiN and trap sites than the distance between the Pt and the traps. In the LRS (panel iv), the asymmetric Schottky barriers induce self-rectification, i.e., electron injection from Pt is much lower than that at the opposite interface. When a negative reset bias is applied on the Pt electrode (panels v and vi), the Fermi level of the Pt electrode is pulled up above the trap levels in TiO_y and NbO_x. Therefore, the Pt electrode can provide the electrons to the trap sites, and the HRS is restored. The electron transport into the trap levels under negative bias was not detectable as a current flow because these electrons do not reach the counter electrode. Meanwhile, this trapping process increases the Schottky barrier height again, suppressing further carrier trapping as well as the leakage current, which is beneficial both for controlling memristor over-reset and leakage current in an array.

To confirm the role of each layer, TiN/20 nm NbO_x/TiN (T-2N), Pt/20 nm NbO_x/TiN (P-2N), and TiN/10 nm NbO_x/2 nm TiO_y/10 nm NbO_x/TiN (T-NTN) devices were prepared through the same fabrication process, and their $I-V$ curves were measured. The results are summarized in Figure 3a. Figure 3b shows schematic illustrations of the conduction behavior of all devices in Figure 3a, where arrows represent the relative conductivity for each electron transport direction. The T-2N device (panel i of Figure 3b) showed a relatively higher and symmetric current conduction due to the symmetric and low Schottky barriers of two TiN−NbO_x interfaces. When the top electrode was replaced with Pt from TiN (P-2N device, panel ii), the $I-V$ curves become asymmetric due to the higher Schottky barrier of the Pt−NbO_x top interface than that of TiN−NbO_x bottom interface. Also, the forward current (electron injection from the bottom TiN) was decreased compared to the T-2N device because the Pt−NbO_x contact increased the overall energy level of the conduction band so the effective Schottky barrier height was increased. The T-NTN device, where a TiO_y layer was effectively inserted into the center of the NbO_x of a T-2N device (T-NTN device, panel iii), also showed a symmetric conduction behavior similar to the T-2N device. This was anticipated from the symmetric device structure, but the overall current level of the T-NTN device was smaller than the T-2N device due to the added TiO_y layer. The upper NbO_x layer also has an appreciable concentration of Ti forming trap sites. The $I-V$ curve of the T-NTN device contained a significant noise component, which could be caused by thermal charge trapping and detrapping in the TiO_y and upper NbO_x layers during the carrier transport measurements. This identified the TiO_y layer as the primary provider of trap sites. Nevertheless, significant resistance switching was not observed clearly because the current level was already quite high due to the low Schottky barrier heights at both interfaces, which dominated the electron trapping. Therefore, the P-NTN device (panel iv) structure was required to simultaneously achieve reproducible resistance switching and self-rectification while also being electroforming-free. The double arrows in panel iii and panel iv of Figure 3b illustrate the current flow in the presence of empty and filled charge traps. In panel iii, charge trapping is negligible so that the forward and reverse currents are symmetric and relatively high. In panel iv, as the electron traps are depleted, the current increases. In summary, the defect levels in TiO_y and Ti impurity centers in the upper NbO_x layer form charge trap centers that exchange electrons with the Pt top electrode via tunneling depending on the bias polarity. Charge trapping during the

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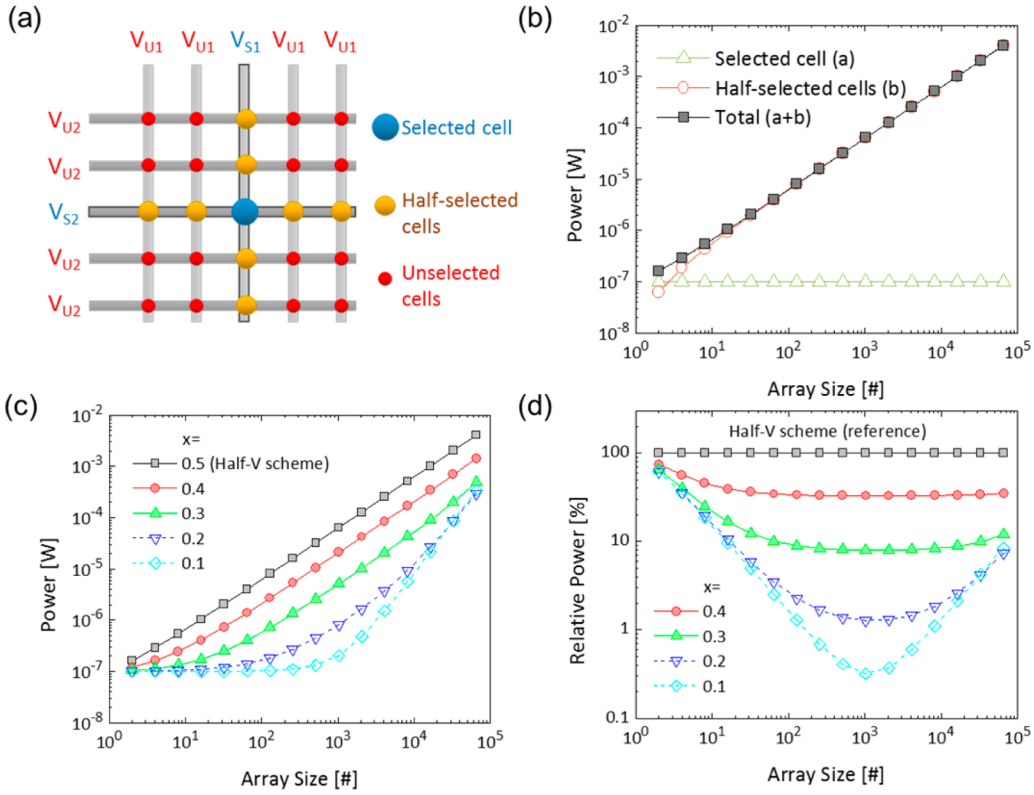

Figure 4. Power consumption calculation for the device in a crossbar array. (a) A schematic of the crossbar array. (b) The power consumption through the selected cell, half-selected cells, and their sum at the half voltage scheme (HVS). (c) The total power consumption at the asymmetric voltage scheme (AVS) as a function of the array size. (d) The relative power consumption of the AVS compared to the HVS.

negative reset bias results in an effective Schottky barrier height increase caused by the negative space charge of the trapped electrons, which creates the HRS. In contrast, a positive set bias on the Pt electrode extracts the trapped electrons and lowers the Schottky barrier, which increases the conductivity of the structure and recovers the LRS. Although this switching model is physically reasonable, further studies are required to confirm it beyond question and therefore, at this stage, it is still a proposal.

As shown in Figures 1b and 1f, this device has two notable characteristics suitable for low-power operation in a crossbar: a low programming current and a high rectifying ratio. The $I-V$ curves in Figure 1b show that the set switching current (I_{SET}) is only 10 nA at a set voltage (V_{SET}) of 10 V, while the reset switching current (I_{RES}) is less than ~1 pA, even at a reset voltage (V_{RES}) of −12 V. Although the switching voltages are high, which could be a burden for the accessing circuit design, the low power ($P = V \times I$) capability acquired by the ultralow switching current is promising for low-power memristor applications. The rectification ratio of this device is at least 10^5 between 10 and −12 V, which can guarantee a low sneak current from the unselected cells. Moreover, the rectifying feature can provide a new capability to reduce the programming power in a crossbar structure by using an optimized biasing scheme as shown below.

In the integrated crossbar structure, even though the programming power for one selected cell is very low as shown in Figure 1b, "sneak current" causes a significant undesirable power consumption.[23,36] Figure 4a shows a schematic diagram of the crossbar array, where a selected cell, half-selected cells, and unselected cells are illustrated as blue, yellow, and red circles, respectively. In this schematic, two selection biases, V_{S1} and V_{S2} are applied on the selected word and bit lines, respectively, to access the selected cell, while two different biases, V_{U1} and V_{U2}, are applied on the other word and bit lines, respectively, to prevent unintentional switching of the half-selected and unselected cells. In this configuration, the total power consumption (P_{TOTAL}) can be simply expressed as follows.

$$P_{TOTAL} = P(V_{S1} - V_{S2}) + (n-1)P(V_{S1} - V_{U2}) + (n-1)P(V_{S2} - V_{U1}) + (n-1)^2 P(V_{U1} - V_{U2}) \quad (1)$$

where $P(V)$ is the power consumption of a memory cell as a function of voltage, and n is the number of word or bit lines in the crossbar array. Here, P_{TOTAL} is calculated under the following conditions; the selected cell is in the HRS and to be programmed to the LRS, while all other cells are in the LRS, which corresponds to the highest power consumption case (the worst case for writing). Other factors that could influence the calculation result, such as the voltage drop along the lines, were assumed to be negligible. A half-voltage scheme (HVS) is one of the common methods in which V_P (programming voltage) and 0 V (ground voltage) are assigned to V_{S1} and V_{S2}, respectively, to apply the programming potential on the selected cell, while a voltage of $0.5V_P$ is applied to all the unselected lines. ($V_{U1} = V_{U2} = 1/2V_P$). This HVS is generally effective for minimizing the total power consumption by eliminating the forth term of eq 1. Under this condition, eq 1 can be simplified as follows.

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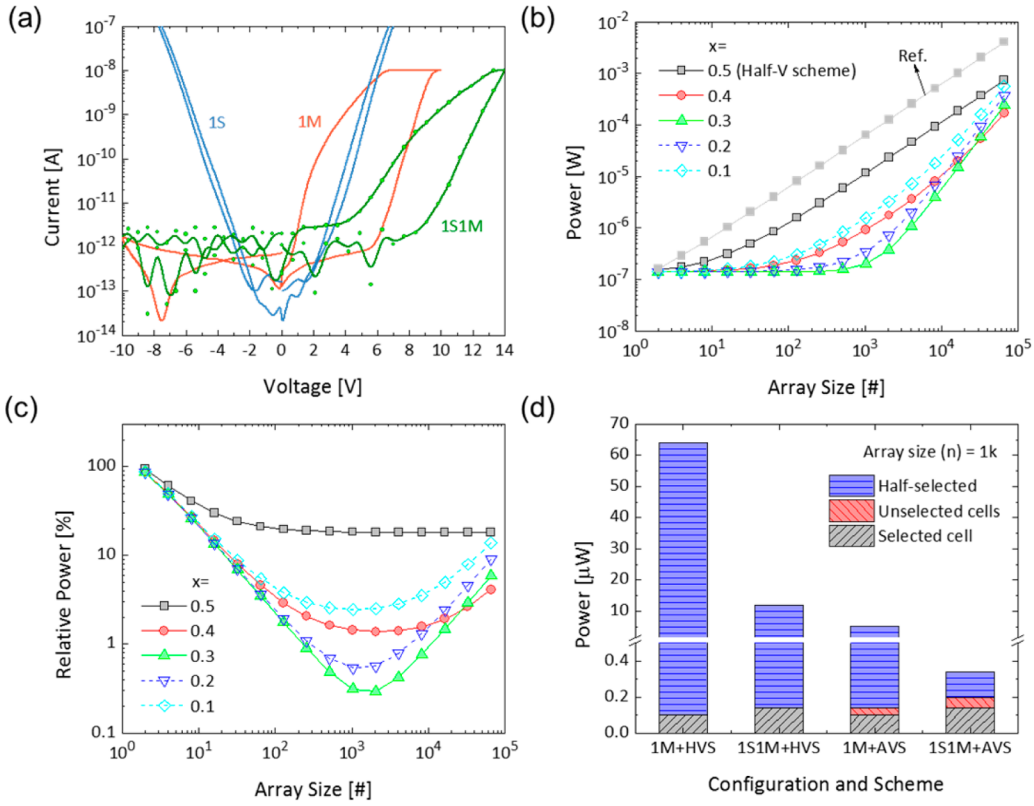

Figure 5. Power consumption with the selector device in the crossbar array. (a) The $I-V$ curves of the memristor (1M), selector (1S), and their series connection (1S1M). (b) The total power consumption of 1S1M at the asymmetric voltage scheme as a function of the array size. (c) The relative power consumption of 1S1M at the asymmetric voltage scheme compare to that of 1 M at the half-voltage scheme. (d) The comparison of the power consumption depending on the biasing scheme and configuration.

$$P_{HVS} = P(V_P) + 2(n-1)P(0.5V_P) \quad (2)$$

In the HVS, the total power consumption (P_{HVS}) is approximately proportional to the array size, n. Figure 4b shows the power consumption calculated from the P-NTN device as a function of array size. The blue triangle, red circle, and black square symbols represent the power consumption of the selected sell, half-selected cells, and their sum, respectively. It is obvious that the power consumption through the half-selected cells becomes much more significant than that through the selected cell as the array size increases. One well-known solution to reduce the sneak power consumption is to adopt a selector component, which has a nonlinear $I-V$ characteristics (low current in low voltage but high current in high voltage) in series with the memristor, where the selector suppresses the sneak currents from the half-selected cells. In addition to the adoption of the selector component, the power consumption can be further decreased by using an optimized "asymmetric voltage scheme" (AVS) that utilizes the self-rectifying feature of the memristor. In the AVS, V_{S1} and V_{S2} are set to V_P and 0 V, respectively, which is identical to HVS. Then, V_{U1} and V_{U2} are set to xV_P and $(1-x)V_P$, respectively, where x is an asymmetry constant from 0 to 0.5 ($0 < x < 0.5$). In the AVS, eq 1 can be rewritten as

$$P_{AVS} = P(V_P) + 2(n-1)P(xV_P) + (n-1)^2P((2x-1)V_P) \quad (3)$$

In the AVS, the half-selected cells experience a smaller voltage than the HVS, and thus, the power consumption through them decreases. However, the unselected cells acquire a negative voltage ($2x - 1 < 0$), so there is additional power consumption through them. Therefore, for the AVS to have an advantage over the HVS ($P_{AVS} < P_{HVS}$), the additional power consumption due to the third term in eq 3 should be smaller than the power saving due to the decreased second term in eq 3. This can be achieved when the memristor has a high rectifying ratio because the current flow via the third term becomes very small. It has to be noted, under this circumstance, the voltage direction for the third term is opposite to the other two terms. The P-NTN device can satisfy this condition. In the device shown in panels b and f of Figure 1, the reverse current is below the sensing level, so it is difficult to estimate an accurate current value in the negative voltage region as a function of voltage. However, considering the fact that the HRS current is proportional to the contact area as shown in Figure 1e, the reverse current level of the 30 nm diameter device must be below 0.01 pA up to the reset voltage of −12 V. (Note that the current of a 700 nm device at −12 V is below 1 pA.) Therefore, a constant 0.01 pA for the reverse current was assumed regardless of the applied negative voltage to simplify the calculation ($I(V < 0) = 0.01$ pA), which is a highly conservative estimation. Figure 4c shows the power consumption as a function of the array size depending on the asymmetry constant, x, and Figure 4d shows the relative power consumption being compared with the HVS (when $x = 0.5$) as a function of the array size. There are certain ranges of array size (n) for smaller total power consumption compared with the HVS. For example, when $x = 0.3$ (so V_{U1} and V_{U2} are 3 and 7 V, respectively, while $V_P = 10$ V), the applied voltage on the half-selected cell and the unselected cells are 3 and −4 V, respectively. In this case, the

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AVS can reduce the power consumption to ~8.0% of HVS at a 1000 × 1000 (= 1 Mbit) array size. At smaller x values than 0.25, the applied voltage on the unselected cell becomes lower than the reset threshold voltage of −5 V, as discussed in Figure 1f, so that this regime is not applicable even though it can provide an even smaller total power consumption ($V_{U1} - V_{U2} < -5$ V when $x < 0.25$).

The benefit of the AVS can be maximized when it is combined with another nonlinear selector. Figure 5a shows the $I-V$ curves of the P-NTN memristor (1M), selector (1S) and their series connection (1S1M), where an in-house nonlinear TaN/TaO_x/TaN selector was used.[37,38] For this demonstration, the S and M are serially connected through external wiring. The $I-V$ curves of the 1S1M configuration showed a higher baseline noise level due to the longer wire connection. However, the serial connection of the S and M showed the desired performance despite the increased noise. When the S was connected, due to the voltage drop across the S, the V_{SET} was increased to 14 V so that the set switching power was increased by 1.4 times for the same set current of 10 nA. However, due to the suppression of the current in the low-voltage region, the power consumption by the half-selected cells can be drastically decreased, and consequently, the total power consumption can be decreased. Figure 5b shows the power consumption from this 1S1M configuration as a function of array size for various x values when $V_P = 14$ V. The reference data of Figure 4b (only M in the HVS) was included for comparison. Figure 5c shows the relative power consumption ratio compared with the reference data. Even for the HVS using 1S1M ($x = 0.5$), the total power consumption was already decreased by ~18% over a wide range of n. When $x = 0.3$ in 1S1M, so V_{U1} and V_{U2} are 4.2 and 9.8 V, respectively, the applied voltage on the half-selected cell and the unselected cells were 4.2 and −5.6 V, respectively. This is one of the safe conditions because the reset threshold voltage decreased due to the voltage drop across the S, the power consumption was drastically decreased to 0.31% of the reference at a 1000 × 1000 array size. Figure 5d summarizes the power consumption through the selected cell, half-selected cells, and unselected cells depending on the above-mentioned schemes (HVS and AVS) and configurations (1M and 1S1M) at a 1000 × 1000 array size. This clearly demonstrates that the selector implementation with the fabricated memristor device under the optimized operation scheme can greatly decrease power consumption in a crossbar.

In this work, the behavior of a low-current and self-rectifying Pt/NbO_x/TiO_y/NbO_x/TiN memristor fabricated over a 30 nm diameter contact via was examined. The device showed a 10 nA set switching current with a ~10^5 rectifying ratio. We have presented a unified model that coherently explains both the resistance switching and the self-rectification of this device in terms of trap-mediated conductance and an asymmetric energy band structure. Our device structure is similar to flash memory, where the charge trapping layer is sandwiched between a tunneling oxide and a blocking oxide. In our device, in the lower NbO_x layer, there are few trap sites, and therefore, it plays the role of a blocking layer. The middle part of the stack (that is, TiO_y/Ti−NbO_x), plays the role of a charge-trapping layer, and the most top portion of NbO_x layer acts as a tunneling oxide. To maximally utilize these features, an asymmetric voltage scheme to bias unselected rows and columns in a crossbar was devised to significantly lower the power dissipation during cell programming. A device with the properties demonstrated here can be used in a 1000 × 1000 crossbar array with AVS to decrease the programming power to 8.0% of the power consumption of a conventional biasing scheme. If the AVS is combined with a nonlinear selector, a power consumption reduction to 0.31% of the reference value is possible. The device presented here shares the charge trapping issue of flash memory so that it also has potential state lifetime limitations. The scaling to extremely small feature size in a crossbar structure may also be limited by charge-induced interference between adjacent cells. The solution for this scaling issue can be adapted from flash memory to make a vertically integrated structure, where the distance between the charge traps can be increased, and therefore, the charge interference problem can be mitigated. Because of the low-voltage operation of our device compared to flash memory, it may find important applications, such as embedded memory on low voltage or power-restricted chips.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b01781.

Figures showing an XPS spectrum of the device, noise currents of the testing tool, read current distribution from 24 cells in two devices, and $I-V$ curves of this device depending on the contact via size and the compliance current. (PDF)

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Notes

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■ REFERENCES

(1) Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. *Nature* **2008**, *453*, 80−83.

(2) Yang, J. J.; Pickett, M. D.; Li, X.; Ohlberg, D. a a; Stewart, D. R.; Williams, R. S. *Nat. Nanotechnol.* **2008**, *3*, 429−433.

(3) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U.-I.; Yoo, I.-K.; Kim, K. *Nat. Mater.* **2011**, *10*, 625−630.

(4) Yang, J. J.; Strukov, D. B.; Stewart, D. R. *Nat. Nanotechnol.* **2012**, *8*, 13−24.

(5) Borghetti, J.; Snider, G. S.; Kuekes, P. J.; Yang, J. J.; Stewart, D. R.; Williams, R. S. *Nature* **2010**, *464*, 873−876.

(6) Jo, S. H.; Chang, T.; Ebong, I.; Bhadviya, B. B.; Mazumder, P.; Lu, W. *Nano Lett.* **2010**, *10*, 1297−1301.

(7) Jo, S. H.; Kim, K.-H.; Lu, W. *Nano Lett.* **2009**, *9*, 870−874.

(8) Kim, K.-H.; Gaba, S.; Wheeler, D.; Cruz-Albrecht, J. M.; Hussain, T.; Srinivasa, N.; Lu, W. *Nano Lett.* **2012**, *12*, 389−395.

(9) Hwang, C. S. *Adv. Electron. Mater.* **2015**, *1*, 1400056.

(10) Yu, S.; Gao, B.; Fang, Z.; Yu, H.; Kang, J.; Wong, H. S. P. *Adv. Mater.* **2013**, *25*, 1774−1779.

(11) Pan, F.; Gao, S.; Chen, C.; Song, C.; Zeng, F. *Mater. Sci. Eng., R* **2014**, *83*, 1−59.

(12) Yang, X.; Chen, I.-W. *Sci. Rep.* **2012**, *2*, 744.

DOI: 10.1021/acs.nanolett.6b01781
Nano Lett. 2016, 16, 6724−6732

(13) Goux, L.; Lisoni, J. G.; Wang, X. P.; Jurczak, M.; Wouters, D. J. *IEEE Trans. Electron Devices* **2009**, *56*, 2363−2368.
(14) Cheng, C. H.; Tsai, C. Y.; Chin, A.; Yeh, F. S. *Technol. Dig. - Int. Electron Devices Meet. IEDM* **2010**, 448−451.
(15) Kang, C.-F.; Kuo, W.-C.; Bao, W.; Ho, C.-H.; Huang, C.-W.; Wu, W.-W.; Chu, Y.-H.; Juang, J.-Y.; Tseng, S. H.; Hu, L.; He, J.-H. *Nano Energy* **2015**, *13*, 283−290.
(16) Jeong, D. S.; Kim, I.; Ziegler, M.; Kohlstedt, H. *RSC Adv.* **2013**, *3*, 3169.
(17) Wu, Y.; Yu, S.; Lee, B.; Wong, P. *J. Appl. Phys.* **2011**, *110*, 094104.
(18) Kim, K. M.; Jeong, D. S.; Hwang, C. S. *Nanotechnology* **2011**, *22*, 254002.
(19) Mehonic, A.; Vrajitoarea, A.; Cueff, S.; Hudziak, S.; Howe, H.; Labbé, C.; Rizk, R.; Pepper, M.; Kenyon, A. J. *Sci. Rep.* **2013**, *3*, 2708.
(20) Patel, N. K.; Nicholls, J. T.; Martn-Moreno, L.; Pepper, M.; Frost, J. E. F.; Ritchie, D. A.; Jones, G. A. C. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1991**, *44*, 13549−13555.
(21) Linn, E.; Rosezin, R.; Kügeler, C.; Waser, R. *Nat. Mater.* **2010**, *9*, 403−406.
(22) Joshua Yang, J.; Zhang, M.-X.; Pickett, M. D.; Miao, F.; Paul Strachan, J.; Li, W.-D.; Yi, W.; Ohlberg, D. a. a.; Joon Choi, B.; Wu, W.; Nickel, J. H.; Medeiros-Ribeiro, G.; Stanley Williams, R. *Appl. Phys. Lett.* **2012**, *100*, 113501.
(23) Kim, G. H.; Kim, K. M.; Seok, J. Y.; Lee, H. J.; Cho, D.-Y.; Han, J. H.; Hwang, C. S. *Nanotechnology* **2010**, *21*, 385202.
(24) Lee, M.-J.; Park, Y.; Suh, D.-S.; Lee, E.-H.; Seo, S.; Kim, D.-C.; Jung, R.; Kang, B.-S.; Ahn, S.-E.; Lee, C. B.; Seo, D. H.; Cha, Y.-K.; Yoo, I.-K.; Kim, J.-S.; Park, B. H. *Adv. Mater.* **2007**, *19*, 3919−3923.
(25) Lee, M.-J.; Seo, S.; Kim, D.-C.; Ahn, S.-E.; Seo, D. H.; Yoo, I.-K.; Baek, I.-G.; Kim, D.-S.; Byun, I.-S.; Kim, S.-H.; Hwang, I.-R.; Kim, J.-S.; Jeon, S.-H.; Park, B. H. *Adv. Mater.* **2007**, *19*, 73−76.
(26) Peng, H. Y.; Li, G. P.; Ye, J. Y.; Wei, Z. P.; Zhang, Z.; Wang, D. D.; Xing, G. Z.; Wu, T. *Appl. Phys. Lett.* **2010**, *96*, 192113.
(27) Guan, W.; Long, S.; Liu, Q.; Liu, M.; Wang, W. *IEEE Electron Device Lett.* **2008**, *29*, 434−437.
(28) Cao, X.; Li, X.; Gao, X.; Yu, W.; Liu, X.; Zhang, Y.; Chen, L.; Cheng, X. *J. Appl. Phys.* **2009**, *106*, 073723.
(29) Kim, K. M.; Choi, B. J.; Lee, M. H.; Kim, G. H.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Han, S.; Hwang, C. S. *Nanotechnology* **2011**, *22*, 254010.
(30) Kim, K. M.; Han, S.; Hwang, C. S. *Nanotechnology* **2012**, *23*, 035201.
(31) Yoon, J. H.; Song, S. J.; Yoo, I.-H.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Hwang, C. S. *Adv. Funct. Mater.* **2014**, *24*, 5086−5095.
(32) Yoon, J. H.; Kim, K. M.; Song, S. J.; Seok, J. Y.; Yoon, K. J.; Kwon, D. E.; Park, T. H.; Kwon, Y. J.; Shao, X.; Hwang, C. S. *Adv. Mater.* **2015**, *27*, 3811−3816.
(33) Cho, E.; Han, S.; Ahn, H.-S.; Lee, K.-R.; Kim, S.; Hwang, C. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2006**, *73*, 193202.
(34) Yu, J.; Yuan, L.; Wen, H.; Shafiei, M.; Field, M. R.; Liang, J.; Yang, J.; Liu, Z. F.; Wlodarski, W.; Motta, N.; Li, Y. X.; Zhang, G.; Kalantar-Zadeh, K.; Lai, P. T. *Nanotechnology* **2013**, *24*, 495501.
(35) Scanlon, D. O.; Dunnill, C. W.; Buckeridge, J.; Shevlin, S. a.; Logsdail, A. J.; Woodley, S. M.; Catlow, C. R. a.; Powell, M. J.; Palgrave, R. G.; Parkin, I. P.; Watson, G. W.; Keal, T. W.; Sherwood, P.; Walsh, A.; Sokol, A. a. *Nat. Mater.* **2013**, *12*, 798−801.
(36) Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Park, T. H.; Kwon, D. E.; Lim, H.; Kim, G. H.; Jeong, D. S.; Hwang, C. S. *Adv. Funct. Mater.* **2014**, *24*, 5316−5339.
(37) Kim, K. M.; Lee, S. R.; Kim, S.; Chang, M.; Hwang, C. S. *Adv. Funct. Mater.* **2015**, *25*, 1527−1534.
(38) Choi, B. J.; Zhang, J.; Norris, K.; Gibson, G.; Kim, K. M.; Jackson, W.; Zhang, M. M.; Li, Z.; Yang, J. J.; Williams, R. S. *Adv. Mater.* **2016**, *28*, 356−362.

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Nano Lett. 2016, 16, 6724−6732